REMARKS/ARGUMENTS

1.) Claim Amendments

The Applicant has amended claims 1-6 and claims 7-26 have been added. Accordingly, claims 1-26 are pending in the application. Support for the new claims can be found throughout the Specification. Applicant asserts that no new matter is contained herein. Favorable reconsideration of the application is respectfully requested in view of the foregoing amendments and the following remarks.

2.) Claim Rejections – 35 U.S.C. § 102(b)

In paragraphs 1-2 of the Office Action, the Examiner rejected claims 1 and 5 under 35 U.S.C. § 102(b) as being anticipated by Fu, et al. (US 5,226,127). Fu teaches the Intel microprocessor and a corresponding co-processor (the '386 processor and '387 math co-processor, as provided on a single chip in the Intel '486 microprocessor, including the pre-fetch circuitry of the '486). In Fu, a 3 clock cycle WAIT instruction is replaced by a one cycle null instruction. In contrast, in the present invention, the first processor is in a sleep state and the second processor is operating independently, whereas in Fu, the microprocessor and co-processor are described as both being in active states (e.g., the microprocessor is not in a sleep state while the co-processor is operating), although the microprocessor of Fu is waiting while the second processor is in operation (See Column 5, lines 1-25 of Fu). Thus, in Fu, there is a dependence of the co-processor on its corresponding microprocessor, whereas in the present invention, the second processor can act independently of the first processor. Also, both the first (host) processor and second (shadow) processor of the present invention operate in parallel, whereas in Fu, the microprocessor is waiting for a signal as when the co-processor has completed its operation (although the number of clock cycles of the wait operation is reduced). Although there are fundamental differences between the present invention and Fu, Applicant has amended Claims 1 and 5 to further emphasize the differences.

Therefore, the allowance of claims 1 and 5 is respectfully requested.

3.) Claim Rejections – 35 U.S.C. § 103(a)

In paragraphs 4-5 of the Office Action, the Examiner rejected claims 2-4 and 6 under 35 U.S.C. § 103(a) as being unpatentable over Fu in view of Kawahara, et al. (US 5,614,847). Kawahara discloses a semiconductor IC adapted to save power by going from an active to an inactive state. Applicant respectfully submits that Kawahara does not remedy the defects of Fu as Kawahara does not teach the ability of second (shadow) processor to operate independently of the first (host) processor. Nevertheless, the Applicant has amended the claims 2-4 and 6 to better distinguish the claimed invention from Fu and Kawahara. Claims 2-4 depend from amended claim 1 and recite further limitations in combination with the novel elements of claim 1. Claim 6 depends from amended claim 5 and recite further limitations in combination with the novel elements of claim 5. Therefore, the allowance of claims 1-6 is respectfully requested.

4.) New Claims 7-26

Claims 7-11

New claim 7 is distinguishable from Fu and is distinguishable from Fu in view of Kawahara. Claim 7 provides for a computer processing arrangement, the arrangement comprising a *host processor*, including a plurality of registers, operable to process instructions from a first set of instructions; and *a shadow processor* operable to access a predetermined, non-zero, selection of the registers and to process instructions from a second set of instructions, which second set of instructions is a subset of the first set of instructions; and wherein the second set of instructions used by the shadow processor is selected from a group consisting of servicing multiple tasks and exceptions, maintaining contexts of the host processor, and controlling interrupts received from peripherals coupled to the computer.

In Fu, the microprocessor and co-processor are described as both being in active states (e.g., the microprocessor is not in a sleep state while the co-processor is

operating), although the microprocessor of Fu is waiting while the second processor is in operation (See Column 5, lines 1-25 of Fu). Thus, in Fu, there is a dependence of the co-processor on its corresponding microprocessor, whereas in the present invention, the shadow processor can act independently of the host processor. Also, both the host processor and shadow processor of the present invention operate in parallel, whereas in Fu, the microprocessor is waiting for a signal as when the co-processor has completed its operation (although the number of clock cycles of the wait operation is reduced). Kawahara does not teach the ability of a shadow processor to operate independently of the host processor. Rather, it teaches the rather simple operation of a semiconductor IC adapted to save power by going from an active to an inactive state.

Claims 8-11 depend directly or indirectly from claim 7 and recite further limitations in combination with the novel elements of claim 7. Therefore, the allowance of claims 7-11 is respectfully requested.

Claims 12-13

New claim 12 is distinguishable from Fu and is distinguishable from Fu in view of Kawahara. Claim 12 provides a method of operating a computer having a *first processor* that operates to process instructions from a first set of instructions, and a *second processor* that operates to process instructions from a second set of instructions, the second set of instructions being a subset of the first set of instructions, the method comprising the steps of using the second processor to receive instructions; and processing the received instructions using the second processor *independently* from the first processor when the received instructions are selected from said second set of instructions, wherein the first processor includes a plurality of registers, and the second processor is operable to access a predetermined, non-zero selection of the registers, and wherein the second set of instructions used by the second processor is one selected from the group consisting of servicing multiple tasks and exceptions, maintaining contexts of the first processor, and controlling interrupts received from peripherals coupled to the computer.

In Fu, the microprocessor and co-processor are described as both being in active states (e.g., the microprocessor is not in a sleep state while the co-processor is operating), although the microprocessor of Fu is waiting while the second processor is in operation (See Column 5, lines 1-25 of Fu). Thus, in Fu, there is a dependence of the co-processor on its corresponding microprocessor, whereas in the present invention, the second processor can act independently of the first processor. Nor does Fu recite the ability of the co-processor to service multiple tasks and exceptions, maintain contexts of the first processor, and control interrupts received from peripherals coupled to the computer. Also, both the first processor and second processor of the present invention operate in parallel, whereas in Fu, the microprocessor is waiting for a signal as when the co-processor has completed its operation. Kawahara does not teach the ability of a second processor to operate independently of the first processor. Rather, it teaches a semiconductor IC adapted to save power by going from an active to an inactive state.

Claim 13 depends from claim 12 and recite further limitations in combination with the novel elements of claim 12. Therefore, the allowance of claims 12-13 is respectfully requested.

Claims 14-26

New claim 14 is distinguishable from Fu and is distinguishable from Fu in view of Kawahara. Claim 14 provides a computer system, having a *host processor*; a *shadow processor* coupled to the host processor, the *shadow processor adapted to control interrupts received from peripherals connected to a computer processor system*; the host processor in communication with an external bus via an external bus interface, the external bus adapted to transfer data to and from a main processor and at least one memory device; a memory controller within the host processor for controlling data access to the at least one memory device; an execution unit for controlling the memory controller and a main processor; an arithmetic logic unit and a plurality of registers within the host processor; the memory controller, arithmetic logic unit and registers and host processor being inter-communication via at least one internal bus; the host processor adapted to process a first set of instructions; the shadow processor adapted

to process a second set of instructions, the second set of instructions being a subset of the first set of instructions; and the *shadow processor adapted to receive control signals and to process instructions in dependence upon those control signals independently of the host processor means*.

In Fu, the microprocessor and co-processor are described as both being in active states (e.g., the microprocessor is not in a sleep state while the co-processor is operating), although the microprocessor of Fu is waiting while the second processor is in operation (See Column 5, lines 1-25 of Fu). Thus, in Fu, there is a dependence of the co-processor on its corresponding microprocessor, whereas in the present invention, the second processor can act independently of the first processor. Fu does not teach the co-processor being adapted to control interrupts received from peripherals connected to a computer processor system, nor does Fu teach the co-processor adapted to receive control signals and to process instructions in dependence upon those control signals independently of its processor. Also, both the first processor and second processor of the present invention operate independently, whereas in Fu, the microprocessor is waiting for a signal as when the co-processor has completed its operation. Kawahara does not teach the ability of a second processor to operate independently of the first processor. Rather, it teaches a semiconductor IC adapted to save power by going from an active to an inactive state.

Claims 15-26 depend directly or indirectly from claim 14 and recite further limitations in combination with the novel elements of claim 14. Therefore, the allowance of claims 14-26 is respectfully requested.

CONCLUSION

In view of the foregoing remarks, the Applicant believes all of the claims currently pending in the Application to be in a condition for allowance. The Applicant, therefore, respectfully requests that the Examiner withdraw all rejections and issue a Notice of Allowance for all pending claims.

The Applicant requests a telephonic interview if the Examiner has any questions or requires any additional information that would further or expedite the prosecution of the Application.

Respectfully submitted,

Date: June 19, 2006

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